CS 631-02 Processer Pesign Components

Projector QiA

Complete Processor Micro architecture

CLM

STATE

STATE

STATE

Design Components

Combinedismal

Logic

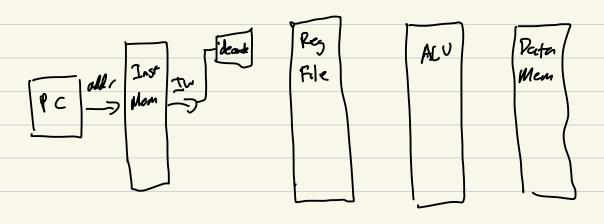
Processor STATE

Posieters

X0-X31

PC

Processo1 Components



Single-cycle processor

X multi-cycle processor

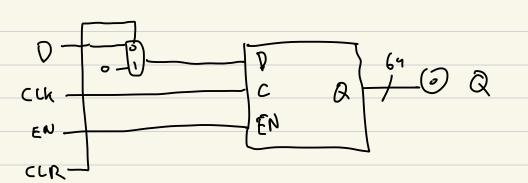
pipelined processor

Moore's Law # of transistors

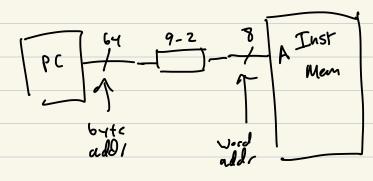
double every 1.5 years

PC Program Counter.

64-6.7 register with CLR (synchronous)



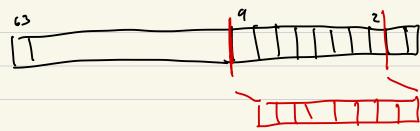
Instruction Memory



word\_addr = byte\_addr /4

= beyte-ald x >> Z

byte adde 67 6:45



Resister File

32 64-lit Registers: xo,x1,...) x31

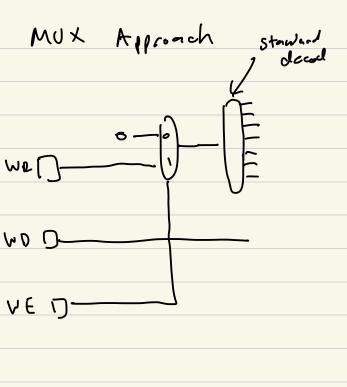
Clend up to two register values and

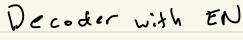
Write up to one register in a sousle

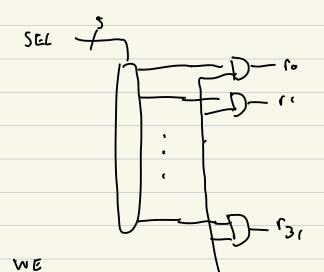
Clock cycle. Xo will always be 0.

5	200 t	RP - readicy H
F PRI	RDO tu	RD - read data
s		WR - write reslates
STONE WE CLE		WP - write duta
WE		WE - write enable
- CLA		

Restricter File Implementation Bto D BAI D Κ, 6 RDO 54032 DXI Pecula EN Q WRD I CLA WD D-WED @ RD1 CLK -4 Q CLR-0 EN CLP







ALU Arithmetic Logic Unit ALU op []