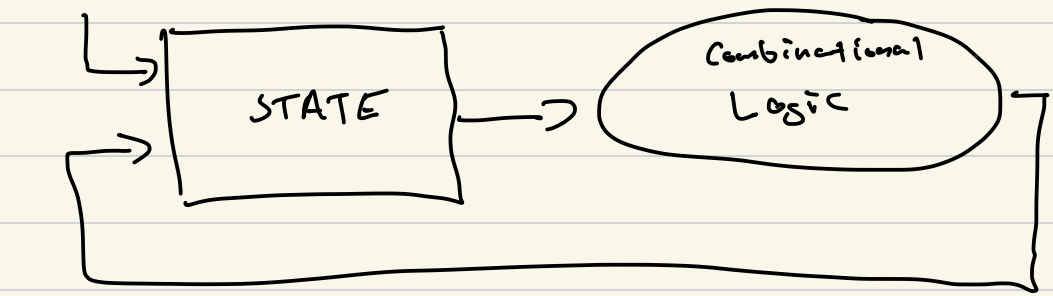
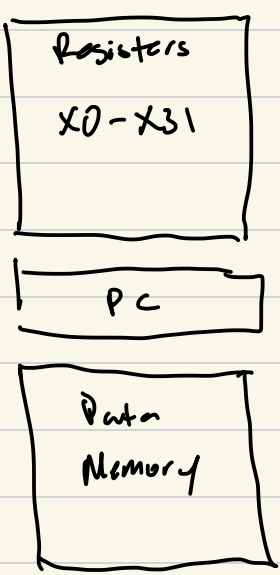
CS 631-02 Processor Design Components

Project 4 Q:A

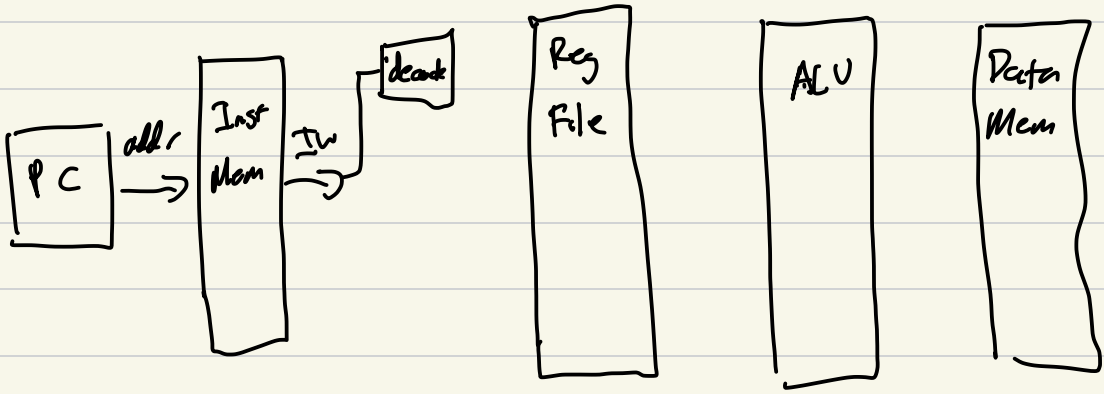
Complete Processor Micro architecture



Processor STATE



Processor Components



Single-cycle processor

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X multi-cycle processor

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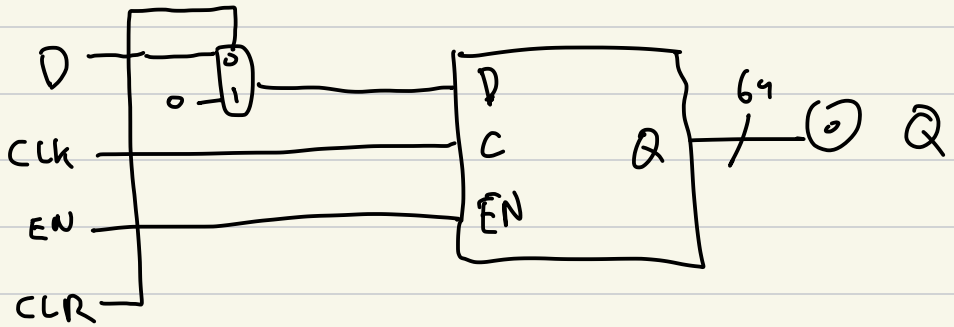
pipelined processor

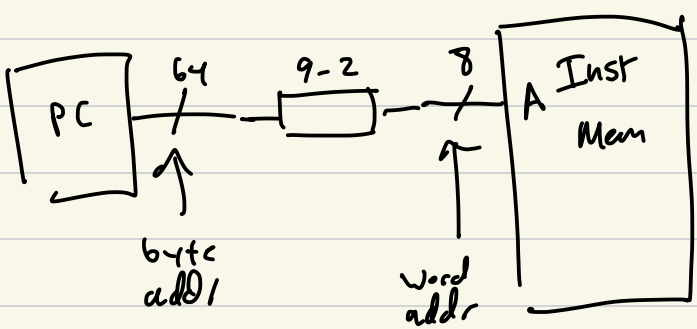
Moore's Law — # of transistors double every 1.5 years

PC Program Counter.

64-bit register with CLR (synchronous)



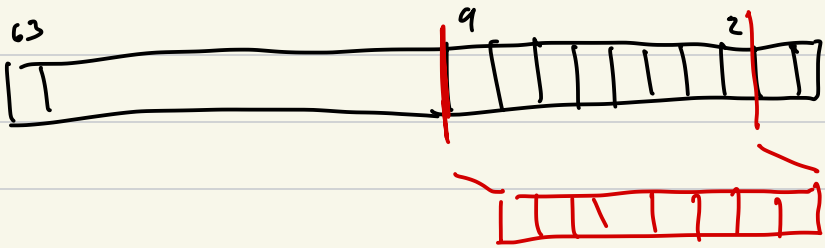
Instruction Memory



word_addr = byte_addr / 4

= byte_addr >> 2

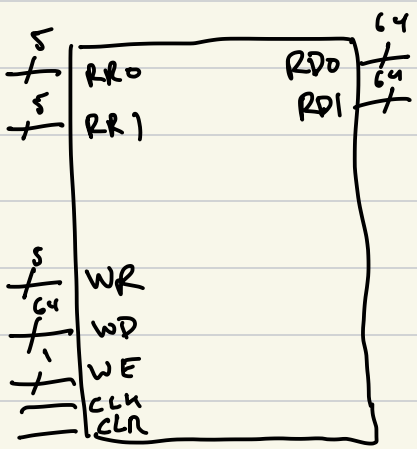
byte addr 64 bits



Register File

32 64-bit Registers: $x_0, x_1, \ldots, x_{31}$

Read up to two register values and write up to one register in a single clock cycle. x_0 will always be 0.



RR - read reg #

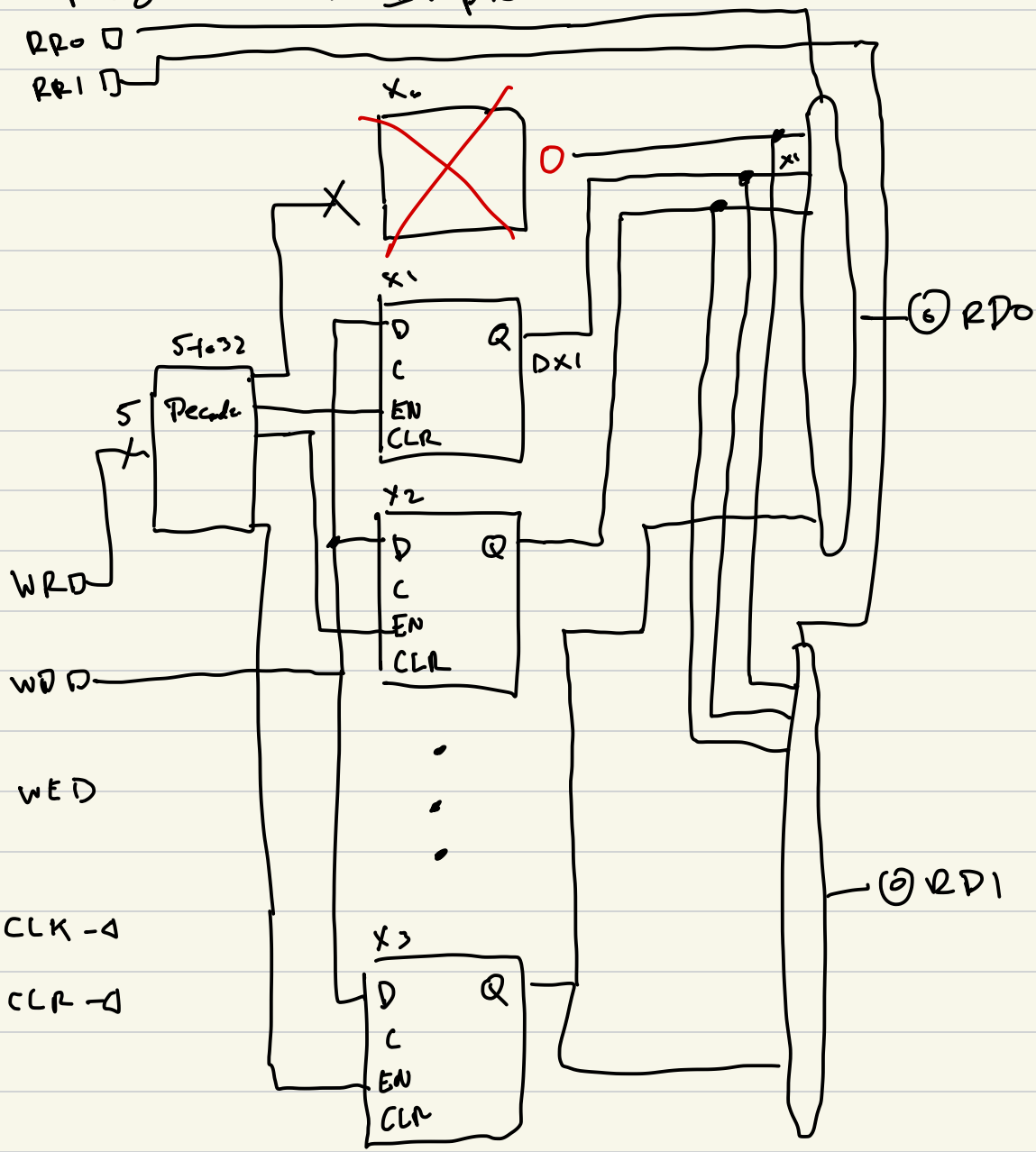
RD - read data

WR - write register

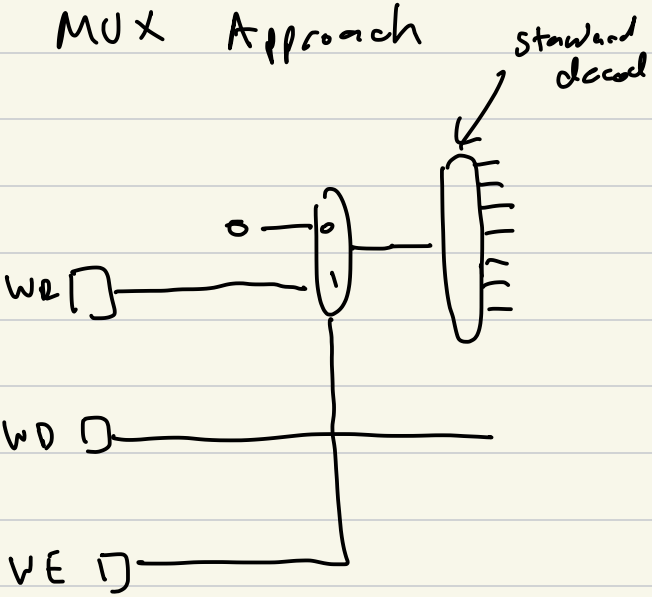
WD - write data

WE - write enable

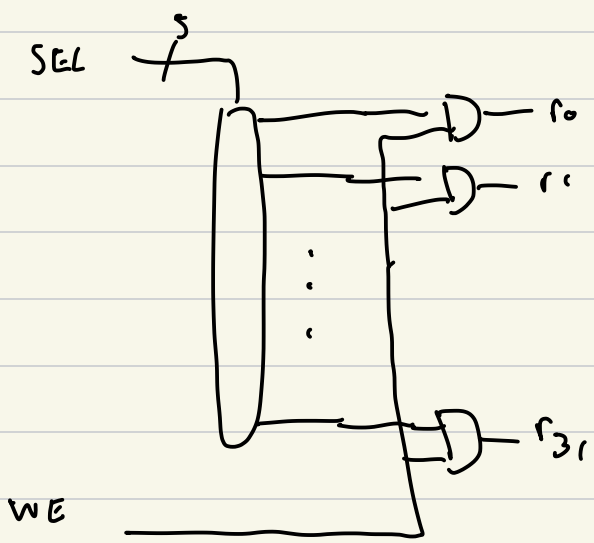
Register File Implementation



MUX Approach



Decoder with EN



ALU Arithmetic Logic Unit